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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/803,350 | 03/08/2001 | Trenton John Grale | 1121-CA | 4188 |

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CIRRUS LOGIC, INC.
CIRRUS LOGIC LEGAL DEPARTMENT
2901 VIA FORTUNA
AUSTIN, TX 78746

| EXAMINER |
|---|
| DINH, PAUL |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 04/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/803,350 | GRALE ET AL. | |
| | Examiner | Art Unit | |
| | Paul Dinh | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

This is a response to the Applicant election with traverse filed on 3/13/03. Because applicant did not distinctly and specifically point out any reasons/grounds/evidences/explanations to support the traverse, the restriction is made final. The applicant is advised that cancellation of non-elected claim(s) is required.

### Specification

a. The specification is objected to because the blank spaces should be filled/updated with US patent applications serial numbers and US patent numbers (if patented). Correction is required.

b. Described element 200C on page 8 is not shown in drawings.

### *Drawings*

a. Figures 2-4, 31 are objected to because the unlabelled blocks should be labeled according to their functions. Correction is required.

b. The drawings filed on 3-8-01 need correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

### *Claim Objections*

Claims 2, 4-5, 10 are objected to because "can" and "can be" are not positive recitations of the invention and should not be used in the claim language. Correction is required.

Claims 7, 9 are objected to because "an input port on said IC to be used to receive different programs for said programmable delta sigma modulator" is not clearly described in the specification.

Claim 11 is objected to because "the circuitry" lacks antecedent basis.

Claim 5 is objected to because this claim does not clearly define what "rates"

Claim 17 is objected to because it should depend from claim 11 to have antecedent basis for "said at least one control signal".

Claims 19-20 are objected to because "two delta sigma modulator, each having an independent controllable output delay" finds no clear support in the specification

*Claim Rejections - 35 USC § 112*

*The following is a quotation of the first paragraph of 35 U.S.C. 112:*
*The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph because claims 1, 4-6, 8 as being a "single means/step" claim, note MPEP 2164.08 (a). Claims 2, 3, 7, 9-20 are rejected because they depend from above-mentioned "single means/step" claims.

*The following is a quotation of the second paragraph of 35 U.S.C. 112:*
*The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.*

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 4, 5, 6, 8 are rejected because the applicant recites the features/functions: "selectable programs (in claim 1)", "programmed for different delta sigma algorithms (in claim 4)", "programmed for different delta sigma rates (in claim 5)"; and "programmable delta sigma modulator (in claims 6, 8), without means or structure in these claims to support these features/functions. Claims 2, 3, 7, 9-20 are rejected because they depend from claims 1, 4, 5, 6, and 8.

Claim 2 is rejected because "N" in "order N" is not clearly defined in this claim.

Claim 15 is rejected because "hybrid memory" is not clearly defined in this claim.

**Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. Claims do not detail invention but claim should clearly define the invention.**

*Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –
*(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*
*(e) The invention was described in-*
*(An application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published*

*under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language;*

1. Claims 1-2, 4-20 are rejected under 35 U.S.C. 102(b) as being anticipated by McGrath et al. (USP 5345409). McGrath discloses a modulator/IC/method method comprising:

(Claim 1) a modulator (120 of fig 1 or c3: 53 or c10: 36+) for receiving sample values and generating digital signals using selectable programs for implementing respective delta sigma algorithms ((fig 1-15, tables 1-5, c18-19) and/or (title/field of invention (programmable DSP) and/or c6: 53-56, c16: 14+, c19: 9+, c21: 55+, c22: 3+)).

(Claim 2) fig 1-15 and/or c19-21 teaches selectable order N.

(Claim 4) an IC (10 of fig 1 or c4: 18+) containing a delta sigma modulator ((120 of fig 1 or c3: 53 or c10: 36+) that [can be] is programmed for different delta sigma algorithms ((fig 1-15, tables 1-5, c18-19) and/or (title/field of invention (programmable DSP) and/or c6: 53-56, c16: 14+, c19: 9+, c21: 55+, c22: 3+)).

(Claim 5) an IC (10 of fig 1 or c4: 18+) containing a delta sigma modulator ((120 of fig 1 or c3: 53 or c10: 36+) that [can be] is programmed for different delta sigma rates ((fig 1-15, tables 1-5, c18-19) and/or (title/field of invention (programmable DSP) and/or c6: 53-56, c16: 14+, c19: 9+, c21: 55+, c22: 3+), see c11 and/or c13-15 and/or claims 1, 6, 10 for "rates").

(Claims 6, 8) a method comprising the step of providing a programmable delta sigma modulator ((fig 1-15, tables 1-5, c18-19) and/or (title/field of invention (programmable DSP) and/or c6: 53-56, c16: 14+, c19: 9+, c21: 55+, c22: 3+)).

(Claims 7, 9) fig 1, 3, 5 teach an input port on IC for receiving different programs for said programmable delta sigma modulator.

(Claim 10) fig 1, 3, 7, 12 or c6-8, 12 and/or tables c16-20 teaches coefficient set(s) selecting.

(Claim 11) fig 1-15 and tables 1-5, c18-19 teach different algorithms are implemented by changing a particular architecture of [the] a circuitry in response to a control signal.

(Claim 12) fig 5-6, 8 and/or 10-12 teaches a multiplier.

(Claim 13) "no multipliers only shifts and adds" is merely and intended use or not use, i.e., shifts and adds perform multiplying function. Just for applicant information, fig 6, 11, 15, c4, table 2 teach shifts and adds

(Claim 14) c11 and/or c14 and/or c21 teach pipeline architecture.

(Claim 15) fig 1, 3-4, 7 teach hybrid memory system.

(Claim 16) fig 1, c12-14, c18 teaches register file arrangement.

(Claim 17) fig 3 teaches a sequencer.

(Claims 18-19) fig 1 shows two delta sigma modulators each having an independently controllable output delay

(Claim 20) fig 15, table 2 teaches controllable delay is a shift register with selectable number of active stages

2. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Keevill et al. (USP 6359938). Keevill discloses a modulator/IC/method method comprising:

(Claim 1) a modulator (fig 17) for receiving sample values and generating digital signals using selectable programs for implementing respective delta sigma algorithms (c13, 22)

(Claim 2) c5-6 and/or c13-16 teaches selectable order N.

(Claim 3) fig 6 and/or 10-11and/or 23 teaches sample values are stored in FIFO elements.

(Claim 4) an IC (title/abstract) containing a delta sigma modulator (fig 17) that [can be] is programmed for different delta sigma algorithms (c13, 22).

(Claim 5) an IC (title/abstract) containing a delta sigma modulator (fig 17) that [can be] is programmed for different delta sigma rates (c13, 22, abstract).

(Claims 6, 8) a method comprising the step of providing a programmable delta sigma modulator (fig 17)

(Claims 7, 9) fig 12, 17 teach an input port on IC for receiving different programs for said programmable delta sigma modulator.

(Claim 10) c4, 6-7 teaches coefficient set(s) selecting.

(Claims 11, 15) fig 1-57 teaches different algorithms are implemented by changing a particular architecture of [the] a circuitry in response to a control signal and hybrid memory.

(Claim 12, 14, 16) abstract/summary teach pipeline architecture, multiplier, register file arrangement.

(Claim 13) "no multipliers only shifts and adds" is merely and intended use or not use, i.e., shifts and adds perform multiplying function. Just for applicant information, summary teach shifts and adds

(Claim 17) fig 14, 16 teach sequencer.

3. Claims 1-2, 4-9, 11-13, 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Engeler (USP 5151970). Engeler discloses a modulator/IC/method method comprising:

(Claim 1) a modulator (c22: 25+) for receiving sample values and generating digital signals using selectable programs for implementing respective delta sigma algorithms (c20: 59+, c22: 25+, claim 5 (algorithms))

(Claim 2) abstract, fig 1-20 teaches selectable order N.

(Claim 4) an IC containing a delta sigma modulator that [can be] is programmed for different delta sigma algorithms (c20: 59+, c22, claim 5)

(Claim 5) an IC containing a delta sigma that [can be] is programmed for different delta sigma rates (c20: 59+, c22, 18+, rates are the conversion speed and/or sampling rates)

(Claims 6, 8) a method comprising the step of providing a programmable delta sigma modulator (c22)

(Claims 7, 9) c8: 10+ teach an input port on IC for receiving different programs for said programmable delta sigma modulator.

(Claims 11, 15) fig -20 teaches different algorithms are implemented by changing a particular architecture of [the] a circuitry in response to a control signal and hybrid memory system.

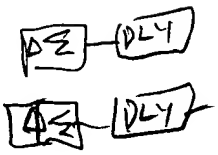
(Claim 12) c11: 34+ teach a multiplier.

(Claim 13) "no multipliers only shifts and adds" is merely and intended use or not use, i.e., shifts and adds perform multiplying function.

(Claim 16) background, fig 2-3, 6-7, 14, 18, teaches register file arrangement.

(Claim 17) fig 11, 15-18 teaches a sequencer.

(Claims 18-19) c22 teach two delta sigma modulators (sigma delta modulator portions of the converter) each having an independently controllable output delay (fig 4, 6-7, 18 digital memory providing delay, c8: 64, delay line memory)




(Claim 20) fig 4, 6-7, 18 teaches controllable delay is a shift register with selectable number of active stages.

4. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Del Signore et al. (USP 5157395). Del Signore discloses an IC containing a delta sigma that [can be] is programmed for different delta sigma rates (abstract, fig 1, c1)

*Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is (703) 305-5662. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (703) 308-1323. The fax number for the organization handling this application is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Paul Dinh
Patent Examiner
April 21, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800